Electrochemical Impedance Spectroscopy and Characterization of 20\% Yttria doped Cerium on Silicon

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Bare silicon and 20\% yttria stabilized ceria on a silicon substrate are annealed. The annealed substrates are analyzed at varying temperatures using electrochemical impedance spectroscopy. The impedance data is fitted against appropriate equivalent circuits and the fitted data is characterized with an Arrhenius plot and a plot of the ionic conductivity against temperature. The 20\% YDC sample is found to have a high ionic conductivity, and therefore should be studied further in order to determine the practicality of using YDC as an electrolyte.

Introduction

Solid Oxide Ceramic Fuel Cells, or SOFCs, are devices that produce energy through oxidizing a fuel. SOFCs have three main components: an anode, a cathode, and an electrolyte. In the cathode, an oxidant, generally oxygen from air, is continuously fed to the cathode and reduced. The oxygen ions travel through the electrolyte to the anode. In the anode, continuously added fuel is oxidized with oxygen ions entering through the electrolyte. Electrons from the anode are transported to the cathode in order to drive the process. SOFCs generally operate at high temperatures of approximately 1000 °C. Lowering the operating temperature of the SOFC would reduce the operating costs and degradation rate of SOFCs, making their use more reasonable.

In order to increase the performance of SOFCs, the components should be optimized. For example, the cathode and the anode of the SOFC should have high electrical conductivity in order for ions to be driven through the electrode.\(^1\) The cathode should be porous in order to allow oxygen molecules to enter the electrode. Therefore using porous materials with increased ionic conductivity can be used in order to increase the performance of the cell. A porous material needs to be used for anode as well as this would allow fuel molecules to enter.

For the electrolyte, the material is an ionic conductor in order to facilitate the transport of negatively charged ions.\(^2\) The electrolyte should also have a low electronic conductivity in order to reduce electricity losses through the electrolyte. Grain boundaries, interfaces between separate grains in crystalline structures, decrease the rate at which ions can travel through an electrolyte, as there is a higher resistance at the grain interfaces than the interior of the grain. Because the grain boundary resistivity hinders the movement of oxygen ions, the grain boundary resistivity should be low.

A widely used and studied electrolyte material is yttria stabilized zirconia (YSZ) as a result of its high ionic conductivity and low electronic conductivity. In this material ZrO\(_2\) molecules are stabilized with the addition of Y\(_2\)O\(_3\).\(^3\) Another much less studied material is yttria doped ceria (YDC). This is created by adding Y\(_2\)O\(_3\) to CeO\(_2\) in order to increase the electrolytes ionic conductivity.\(^4\)

For solid electrolytes, the conformation of the solid impacts the ionic conductivity. This concept is the building block behind the use of YSZ as an electrolyte. At room temperature, ZrO\(_2\) holds a monoclinic structure.\(^4\) In a monoclinic structure, ions have the ability to travel through the material in multiple directions and each path has a different length. This structure is inefficient as the ions may, as a result, go through longer paths in order to travel through the electrolyte. If Y\(_2\)O\(_3\) is added to the ZrO\(_2\), the zirconia may be stabilized into the cubic or tetragonal structure. These structures are more favorable as they lessen the distance that the ions need to move. For the cubic structure, all the directions that the ion may travel have sides of equal length. This lessens the overall distance that ions travel and is the reason that Yttria Stabilized Zirconia is used rather than pure ZrO\(_2\).

Another material that may be used as an electrolyte is yttria doped cerium (YDC). At the operating temperatures of an SOFC, cerium has a cubic structure and does not need Y\(_2\)O\(_3\) for stabilization. Y\(_2\)O\(_3\) is added to the ceria in order to increase the electrolyte’s ionic conductivity. Y\(_2\)O\(_3\) causes oxygen vacancies to develop. These vacancies allow a larger amount of oxygen ions to pass through the YDC matrix.\(^5\)

In our experiment we will be furthering research on YDC as a possible electrolyte by testing the electrochemical properties of YDC. The impedances of bare silicon and YDC on silicon will be examined in order to understand which effects originate from YDC and which originate from Silicon. From this data, the relationship of the resistivity and ionic conductivity with temperature can be determined.

Methods

Impedance Spectroscopy

Electrochemical impedance spectroscopy is used in the measurements and analysis of materials for which ionic conduction dominates. Using an applied potential, the
impedance is measured and analyzed. The method with which the electrolyte is measured depends on the phase and properties of the electrolyte. For solid electrodes, impedance is measured using two parallel electrodes on the same plane. The response of the can then be displayed and analyzed with analytical software. The response is plotted on a three dimensional plot with axes of the log of frequency, the real impedance and imaginary impedance. This three dimensional plot can then be separated into a Bode impedance plot and a Nyquist Impedance plot. The impedance data can then be analyzed and fitted to an Equivalent circuit, dependent on the examined material.

Experimental Setup

A 100 nm sample of bare silicon doped with boron is annealed at 700°C for 10 minutes under flow of helium and then cooled to room temperature. Two parallel electrodes are pasted onto the sample using high temperature silver paste (Heraeus C8729- conductor paste). Immediately after annealing each sample, the impedance of the sample is measured using electrochemical impedance spectroscopy (EIS). The sample is placed in an enclosed chamber and the impedances are measured with a potentiometer. The impedance of the samples are measured at room temperature and then the temperature is incrementally increased to 600 °C.

Yttria doped ceria films are deposited on silicon using the precursors tris(isopropyl-cyclopentadienyl) Cerium maintained at 120 °C , and tris (isopropyl-cyclopentadienyl) Yttrium maintained at 110 °C as well as water vapor. Six silicon substrates were cut into 1.5 cm by 1.5 cm squares and cleaned. The cleaned samples are placed in the reactor chamber and the metal precursors are added into the reactor.

Six samples of 45 nm 20%YDC on 100nm samples of silicon doped with boron are annealed at 700°C for 10 minutes under flow of helium and cooled to room temperature. After annealing each sample, the samples were analyzed with electrochemical impedance spectroscopy using a Bio-Logic SP-240 potentiostat. 10 mV AC digital amplitude is used. The sensors are placed on the sample using high temperature silver paste. The impedances are measured at room temperature and as the temperature is incrementally increased to 600°C.

The impedance data is recorded and analyzed using E.C. lab, an EIS software. The Nyquist impedance and Bode impedance plots are then fitted against an equivalent circuit so that the sample may be analyzed. The Bode Impedance plot is a graph of the absolute value of impedance and the phase of the impedance with respect to the frequency. The Nyquist impedance plot shows a graph of the imaginary impedance plotted against the real impedance.

Determining the Equivalent Circuits

For the impedance plots of each sample to be analyzed, they can be fitted against an appropriate equivalent circuit. The equivalent circuit used to fit the Bare Silicon Impedance plots is shown in Figure 1, where R1 and R2 represent resistors and C1 represents a capacitor. The R1 represents the resistivity resulting from the potentiometer. The R1/C1 section represents interfacial diffusion of oxygen molecules.

![FIG. 1: Equivalent Circuit of Bare Silicon](image1)

The equivalent circuit of 20% atom YDC on silicon has to include the effect of the grain boundary resistivity throughout the electrolyte as well as the effect of oxygen ions transporting through the YDC. The resulting equivalent circuit is shown in Figure 2, where R1, R2, R3, and R4 are resistors; C1, C2 and C3 are capacitors; and Q1 is a constant phase element. R1 represents the effects of the potentiostat and (Q1+C2/(R3)) represents the effects of the grain boundary. C1/R2 represents the interfacial oxygen diffusion on the face of the electrolyte and C3/R4 represents the movement of oxygen ions through the YDC matrix.

![FIG. 2: Equivalent Circuit of 20% YDC on Silicon](image2)

Results and Discussion

Silicon Impedance Trends

After the impedances of the bare silicon samples at differing temperatures were recorded, they were fitted against the stated equivalent circuit. The fits were found to be accurate representations of the experimental data as shown in Figure 3. No grain boundary is present.

When the Nyquist plots of bare silicon samples of differing temperatures are compared, as shown in Figure 4, two trends transpire. From 100 °C to 300 °C the impedance of the samples decrease and from 350 °C onward the impedance increases.
FIG. 3: Nyquist impedance plot of bare silicon measured at 100 °C. The red points correspond to the fit created by the equivalent circuit while the blue points correspond to the experimental data.

FIG. 4: Fitted Nyquist Impedance plots for Bare Silicon tested from 100 °C to 400 °C.

The change in the relationship between temperature and impedance for the samples is likely a result of boron doped silicon acting as a semiconductor.

20% YDC Characterization

After the impedances of 20% YDC on silicon at differing temperatures is recorded, the plots were fitted to the stated equivalent circuit. The fits were found to be accurate as shown in Figure 5. The grain boundary resistivity is suggested by the graph as there are two maxima in the Nyquist plot. The first maxima corresponds to the grain boundary resistivity.

The ionic conductivity of each 20% YDC sample was plotted against temperature. The equation used to find the conductivity at each temperature is

$$\sigma = \frac{d}{S \cdot R}, \quad (1)$$

where $\sigma$ is the ionic conductivity at a certain temperature, $d$ is the thickness of the sample, $S$ is the surface area of the sample, and $R$ is the total resistance calculated through the equivalent circuit. The data is plotted against temperature and fitted to an exponential function in Figure 6. The equation of the fitted plot is $y = 2 \cdot 10^{-14} e^{0.0227x}$. The surface area of the sample is 1.62 cm and the thickness of the sample is 40 nm.

The ionic conductivity is a key property for electrolytes and therefore the trend for the increase of Ionic conductivity with increasing temperature must be understood. A good electrolyte must have a high Ionic conductivity. Thus this relation can be used to determine the approximate Ionic conductivity of the electrolyte at SOFC operating temperatures and to compare 20% YDCs Ionic conductivity with other material when choosing an appropriate electrolyte.

Arrhenius Plot

The Arrhenius plot of the 20% YDC samples was plotted against 1000/Temperature as shown in Figure 7. The equation for the Arrhenius plot is

$$\sigma T = A \times e^{-\frac{E}{RT}}, \quad (2)$$

where $E$ is the activation energy, $k$ is the rate constant, $T$ is absolute temperature and $A$ is a pre-exponential factor. The linear regression equation for the data from 373 K to 523 K is $-6.244 T + 6.208$. The linear regression equation for the data from 573 K to 673 K is $-3.827T + 1.695$.

The linear regression used to fit the data of the Arrhenius plot changes after 523 K. The reason for this change...
is that, as stated earlier, the impedance of the silicon base, which is contingent on the resistivity, has a changing correlation with temperature. The conductivity of a material is directly calculated from the resistivity system. Therefore the linear regression must be changing where the relation between impedance and temperature changes. According to the Nyquist Impedance graphs, this change occurs between 523 K and 573 K.

FIG. 6: Graph of the total ionic conductivity of 20% YDC samples against temperature. The diamond markers are the calculated data. The black line corresponds to the fitted exponential plot.

FIG. 7: Arrhenius plot for 20% YDC samples from 373 K to 673 K. Blue points correspond to the calculated data. The red line corresponds to the linear regression for 573K to 673K and the light blue line corresponds to the linear regression for 373 K to 523 K.

Conclusion

The experimentally collected impedance spectroscopy data for YDC on silicon and bare silicon was fitted using equivalent circuits dependent on the properties of the samples. These equivalent circuits accurately represented the experimental data. The fitted Nyquist Impedance plots for bare-silicon showed that Impedance decreased with the T from approximately 100 °C to 300 °C and then began increasing with temperature.

For YDC, the ionic conductivity increases with temperature. The relationship for ionic conductivity and absolute temperature can be modeled with an exponential function. The Arrhenius plot showed a change in behavior near 300 °C from a small slope to a steeper slope.

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4 Structure and phase relationship of cubic zirconium dioxide (1975).
6 M. Krauz, M. Radecka, and M. Rękas, Materiały Ceramiczne 63, 157 (2011).